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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/340,776	06/28/1999	GAJINDER SINGH PANESAR	S1022/8250	4340

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JAMES H MORRIS
C/O WOLF GREENFIELD & SACKS PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 022102211

EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/340,776	Applicant(s) Gajinder Singh Panesar
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 16, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *1-5* is/are allowed.

6) ☒ Claim(s) *6 and 7* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Aug. 16, 1999* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is response to applicant remarks filed July 16, 2002. Claims 1-7 are pending in this official action.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The formal drawing, filed on Aug. 16, 1999 have been received and entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Aleksic et al., Patent no. 5,995,736.

As per claim 6, Aleksic anticipated method and system for simulating integrated circuit including ASIC design or application specific processor (ASP) identical to the claimed invention (Abstract and Summary of the Invention). According to Aleksic, the simulation system includes

means for defining functional model for the processor (col. 2, lines 45-56, col. 4, line 1-53, col. 5, lines 18-31), means for simulating functional model based on hardware design and outputting result of simulation, means for converting result of hdl functional model simulation into a simulation language such as C/C++, for instance (col. 5, line 8 to col. 6, line 6, line 56) and means for simulating the circuit design at circuit level for subsequent simulation phase (col. 5, lines 37-67, col. 7, lines 40-60, col. 8, lines 8-60).

As per claim 7, claim 7 is directed to computer program product for performing steps for the system claim 6 above, and Aleksic anticipated computer program product including modeling file as claimed (Abstract and Summary of the Invention). According to Aleksic, the simulation system includes program product means for defining functional model for the processor (col. 4, line 30-65), a program product for simulating functional model based on hardware design (col. 2, lines 45-56, col. 4, lines 30-65, col. 5, lines 18-31), programming means for generating interface function file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface for subsequent circuit level simulation (col. 5, lines 55-67, col. 7, lines 40-60), program means for simulating in the high level language as part of the functional model an application executable by the CPU, including for a predetermined simulation phase, test function files, and operation of the set of peripheral devices, outputting the state of the application and the state of the peripherals to the modeling file for converting the modeling file in the high level programming language to a language executable by the simulation system (Figs. 2-4, col. 4, lines 48-65, col. 5, lines 18-31, col. 6, lines 15-35, cols. 7-8), means for converting result of hdl functional model simulation into

a simulation language such as C/C++ for instance (col. 5, line 8 to col. 6, line 56), and means for simulating the application specific integrated circuit design as claimed.

Allowable Subject Matter

5. Claims 1-5 are allowed. The following is an examiner's statement of reasons for allowance: the claimed invention is method and system for simulating integrated circuit including ASIC design or application specific processor (ASP). The simulation system includes means and functional steps for defining functional model for the processor, means for simulating functional model based on hardware design, generating interface function file for hardware interface which defines the communication of the peripheral with the processor, simulating in the high level language as part of the functional model an application executable by the CPU, including for a predetermined simulation phase, test function files, and operation of the set of peripheral devices, outputting the state of the application and the state of the peripherals at the end of a predetermined simulation phase to a modeling file in the high level language and converting the modeling file in the high level programming language to a language executable by the simulation system, means for converting result of hdl functional model simulation into a simulation language, for simulating , and means for simulating the application specific integrated circuit design as claimed. The art of record does not expressly disclose such feature limitations as in claims 1-5.

Response to Arguments

6. Applicant's arguments filed 01/30/2002 have been fully considered but they are not persuasive.

In response to applicant's remark Aleksic fails to disclose or suggest means for simulating an ASP in which the state of the functional model at the end of a simulation phase is used to simulate the ASP at circuit level (page 4, paragraph 1), the examiner disagrees with. Alexic anticipates system for simulating application specific processor in subsequent phase of circuit level simulation (col. 4, lines 48-65, col. 5, lines 37-67). In other words, ASP simulation files have been used for subsequent simulation or emulation at the circuit level for simulation of peripheral devices for example as claimed.

In response to applicant's argument Aleksic fails to disclose or suggest using state of the simulation of the functional model to simulate the ASP at the circuit level in a subsequent simulation phase (page 4, last paragraph), the examiner disagrees with. Alexic discloses functional model and its states has been used to simulate the ASP at the circuit level in a subsequent simulation phase such as for emulation of functional requirement of the ASIC (col. 5, lines 55-67) or circuit level in a subsequent simulation phase as applicant's argument in here.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for Formal communications; please mark "EXPEDITED PROCEDURE"),

Or:

(703) 746-7239 (for Unofficial Fax communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

October 17, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER